AMENDMENT TO THE CLAIMS

Please amend claims 1, 12, and 18 as follows:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A method of fabricating a semiconductor structure, comprising:

forming a gate at least partially overlapping at least one source/drain region;

forming a first step of material adjacent a side edge of the gate, which is separated from a gate insulation layer beneath the gate, and forming a second step of material raised above the first step and remote from the side edge of the gate in a single material formation process; and

forming a silicide on the second step and the gate.

2. (Previously presented) The method of claim 1, further comprising depositing sidewalls on the side edge of the gate.

3. (Original) The method of claim 2, further comprising etching a lower portion of the sidewalls to form an undercut.

4. (Original) The method of claim 3, wherein the etching comprises an isotropic etching.

5. (Original) The method of claim 3, further comprising forming the first step at least partially in the undercut.

6. (Original) The method of claim 4, wherein forming the first step and the second step comprises growing the first step and the second step.

7. (Original) The method of claim 2, wherein the second step is formed proximate to the

sidewalls and remote from the gate.

8. (Canceled).

9. (Original) The method of claim 1, wherein the first step is electrically connected with a portion of a conductive region arranged underneath the gate.

10. (Original) The method of claim 1, wherein the first step is spaced away from the side edge by a spacer.

11. (Original) The method of claim 1, wherein the first step and the second step are doped to form a raised source/drain region.

12. (Currently Amended) A method of forming a source/drain for a semi-conductor device, comprising:

forming a first conductive region on a substrate adjacent a side of a gate ~~and~~, which is separated from a gate dielectric arranged beneath the gate; and

forming a second conductive region at a height above the first conductive region,

wherein the first conductive region and the second conductive region are formed in a single growing step.

13. (Original) The method of claim 12, further comprising arranging the first and second conductive regions above a third conductive region disposed within a substrate.

14. (Original) The method of claim 12, wherein the first conductive region is at a height of approximately 10 nm and the second conductive region is at a height above approximately 30 nm.

15. (Original) The method of claim 12, further comprising forming a spacer between a sidewall of the gate and at least a portion of the first conductive region.

16. (Previously presented) The method of claim 12, further comprising the steps of:

forming at least one sidewall adjacent the gate; and

etching a lower portion of the at least one sidewall to form an undercut,

wherein the first conductive region is formed at least partially within the undercut.

17. (Canceled).

18. (Currently Amended) A semiconductor structure, comprising:

a gate arranged to at least partially overlap at least one source/drain region;

a first step raised above a lower surface of the gate, which is separated from a gate dielectric layer arranged beneath the gate;

a second step, formed in a single growing step with the first step, raised above the first step; and

a conductive layer arranged on a surface of the second step.

19. (Original) The structure of claim 18, wherein the first step is approximately 10 nm high.

20. (Canceled).

21. (Original) The structure of claim 18, wherein a transition between an edge of the second step and the first step is a shape comprising one of a curved portion, an angled portion, and a stepped feature.

22. (Canceled).

23. (Previously presented) The structure of claim 18, further comprising the first step being arranged at least partially under an undercut formed in sidewalls adjacent the gate.